**ABSTRACT**

In this paper some new multilevel inverter topologies, their characteristics and also block diagram are presented. They are essentially based on cascade multilevel inverter with the same number of switches and separated dc sources. The paper is illustrated that increasing the number of output waveform levels in the topologies reduces the low order harmonics and also the total harmonic distortion which are so harmful and trouble maker in power electronic devices. It's shown that one of the presented multilevel inverter topologies uses a method which reduces the number of in use switches. The effect of higher DC link voltage on multilevel inverters is also explained. A new topology of multilevel inverter is presented too which has the highest number of output voltage levels due to the number of the cells which is made it so operational. The topologies MATLAB simulation comparison results are presented as well.

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**List of abbreviations**

|  |  |  |
| --- | --- | --- |
| **S.no** | **Name** | **Abbreviations** |
| 1 | PD | Phase Disposition |
| 2 | NTV | Nearest Three Space Vector States |
| 3 | PWM | Pulse Width Modulation |
| 4 | CSV | Centred Space Vector |
| 5 | VSC | Voltage Source Converter |
| 6 | CSC | Current Source Converter |
| 7 | THD | Total Harmonic Distortion |
| 8 | SDCS | Separate DC Sources |
| 9 | RCT | Reverse Conducting Thyristors |
| 10 | SHE | Sub Harmonic Elimination |
| 11 | SHM | Selected Harmonic Minimisation |
| 12 | IPD | In Phase Disposition |
| 13 | POD | Phase Opposition Disposition |
| 14 | APOD | Alternative Phase Opposition Disposition |
| 15 | NW | Normalized Weighted |
| 16 | PSC | Phase Shifted Carrier |
| 17 | EMI | Electro Magnetic Interference |
| 18 | CSF | Constant Switching Frequency |
| 19 | VSF | Variable Switching Frequency |
| 20 | FPGA | Field Programmable Gate Array |
| 21 | SFO | Switching Frequency Optimal |
| 22 | API | Application Program Interface |